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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

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clock | BUFGP | 104 |

m1/temp1<8> | NONE(Madd\_n00701) | 2 |

w<1><9> | NONE(mr\_Mram\_memory633)| 632 |

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INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer\_type constraint in order to insert these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: 15.154ns (Maximum Frequency: 65.989MHz)

Minimum input arrival time before clock: 4.848ns

Maximum output required time after clock: 3.597ns

Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clock'

Clock period: 15.154ns (frequency: 65.989MHz)

Total number of paths / destination ports: 146458 / 501

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Delay: 15.154ns (Levels of Logic = 3)

Source: m6/Maddsub\_n0019 (DSP)

Destination: y\_t\_0 (FF)

Source Clock: clock rising

Destination Clock: clock rising

Data Path: m6/Maddsub\_n0019 to y\_t\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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DSP48A1:CLK->P17 3 1.200 0.650 m6/Maddsub\_n0019 (m6\_y2<17>)

DSP48A1:B17->P17 1 3.123 0.579 Madd\_n00701 (n0070<17>)

DSP48A1:B17->P7 1 3.123 0.580 Madd\_m9\_y2[17]\_m3\_y2[17]\_add\_20\_OUT1 (m9\_y2[17]\_m3\_y2[17]\_add\_20\_OUT<7>)

LUT3:I2->O 1 0.205 0.000 y\_t\_7\_glue\_set (y\_t\_7\_glue\_set)

FDR:D 0.102 y\_t\_7

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Total 15.154ns (13.345ns logic, 1.809ns route)

(88.1% logic, 11.9% route)

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Timing constraint: Default OFFSET IN BEFORE for Clock 'clock'

Total number of paths / destination ports: 110 / 110

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Offset: 4.848ns (Levels of Logic = 2)

Source: reset (PAD)

Destination: mr/address\_0 (FF)

Destination Clock: clock rising

Data Path: reset to mr/address\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 73 1.222 1.700 reset\_IBUF (reset\_IBUF)

LUT4:I3->O 32 0.205 1.291 mr/address\_val321 (mr/address\_val)

FDR:R 0.430 mr/address\_0

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Total 4.848ns (1.857ns logic, 2.991ns route)

(38.3% logic, 61.7% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'clock'

Total number of paths / destination ports: 8 / 8

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Offset: 3.597ns (Levels of Logic = 1)

Source: y\_t\_7 (FF)

Destination: y<7> (PAD)

Source Clock: clock rising

Data Path: y\_t\_7 to y<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FDR:C->Q 1 0.447 0.579 y\_t\_7 (y\_t\_7)

OBUF:I->O 2.571 y\_7\_OBUF (y<7>)

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Total 3.597ns (3.018ns logic, 0.579ns route)

(83.9% logic, 16.1% route)

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Cross Clock Domains Report:

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Clock to Setup on destination clock clock

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| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

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clock | 15.154| | | |

w<1><9> | 7.712| | | |

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Clock to Setup on destination clock m1/temp1<8>

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| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

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clock | 11.144| | | |

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Clock to Setup on destination clock w<1><9>

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

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clock | 4.226| | | |

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Total REAL time to Xst completion: 136.00 secs

Total CPU time to Xst completion: 135.59 secs

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Total memory usage is 299180 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 28 ( 0 filtered)

Number of infos : 7 ( 0 filtered)